An Active Quenching Circuit for a Native 3D SPAD Pixel in a 28 nm CMOS FDSOI Technology

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Abstract—The first Active Quenching - Active Reset (AQAR) circuit for a novel inherent 3D SPAD pixel is designed in a 28 nm CMOS Fully Depleted Silicon On Insulator (FDSOI) technology. Thanks to an ultra-fast detection circuit, the avalanche is detected in less than 50 ps and quenched in 200 ps. Thanks to this fast detection and active quenching, the avalanche charge in the Space Charge Region (SCR) is reduced by 50 % which should result in a 50 % afterpulsing reduction. With the proposed pixel, the fill factor is no longer limited by the associated circuitry.

Keywords—SPAD pixel, afterpulsing, avalanche charge, active quenching, fast detection, native 3D, CMOS FDSOI.

I. Introduction

Single Photon Avalanche Diodes (SPADs) have a wide range of applications, from biomedical imaging to autonomous vehicles industry. Due to its ability to detect weak light down to a single photon with a good timing accuracy, SPAD is used in Fluorescence Lifetime Imaging Microscopy, Light Detection and Ranging, Time-Correlated Single Photon Counting, 3D imaging, noninvasive VLSI circuits testing and many other applications [1][2].

Beside its advantages, SPAD suffers from two main noise sources, the Dark Count Rate (DCR) and the After Pulsing effect (AP). DCR is defined as the number of non-photo-generated avalanches when SPAD is placed in a complete darkness. The DCR is an uncorrelated noise, mainly caused by tunneling and thermally generated carriers. On the other side, the AP is a noise correlated to the signal. Indeed, when an avalanche occurs, some of carriers that flow through the Space Charge Region (SCR), are captured by traps inside the SCR. These traps release carriers after a random time, which generates spurious avalanches correlated to the previous main avalanche. DCR and AP degrade the SPAD maximal achievable signal to noise ratio [3].

A conventional solution to mitigate DCR, is cooling down the SPAD in order to reduce the thermal generation. However, on the other hand, increasing the temperature, makes trapped carriers to be released faster which results in after pulsing reduction [3]. Another way to reduce the AP is to increase the time interval between avalanches, in which the SPAD is biased out of its breakdown region (dead time). However, increasing the dead time, decreases the counting rate and so the dynamic range. Even though a clean semiconductor fabrication process, decreases the AP effect, many circuit solutions are also proposed to reach that goal. All these solutions are based on this fact that the AP effect is proportional to the number of trapped carriers. Therefore, an Active Quenching (AQ) circuit, that is able to lessen the avalanche charge within the SCR, and thus the number of trapped carriers, is expected to reduce the AP effect [4][5].

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However, the peripheral circuitry required in these methods, reduces the pixel fill factor (the ratio between the SPAD active area and the total pixel area), increases the pixel pitch and consequently degrades the Photon Detection Efficiency (PDE). To overcome these tradeoffs, the 3D stacked structure, micro lenses and even a larger SPAD active area are proposed. In the 3D stacked structure, two separate dies, one hosting the SPAD and other one hosting electronics, are stacked together to increase the fill factor. This solution is costly and complex [1][6].

In this paper, we propose to take benefit of the Fully Depleted Silicon On Insulator (FDSOI) technology to design a native 3D pixel structure [7], including a novel ultrafast active quenching circuit, all in a single die, capable of achieving a high fill factor. The proposed pixel breaks the tradeoff between the AP effect and the fill factor. The pixel is designed in a 28 nm CMOS FDSOI technology in which the transistors are fabricated over an ultrathin buried oxide layer [8]. The oxide layer allows the integration of the electronics over the SPAD, (Fig. 1). This novel pixel structure paves the way for high density and high resolution smart SPAD arrays. Also, thanks to the buried oxide layer, the body biasing feature leads to a new avalanche sensing technique [9][10].

II. SPAD Pixel in FDSOI: a Native 3D Pixel

Fig. 1 illustrates a symbolic cross section of the inherent 3D SPAD pixel, in a CMOS FDSOI technology. The SPAD is realized at the junction of P-well and deep N-well, beneath the thin buried oxide layer. The associated electronics are fabricated in an ultrathin silicon film and placed on top of the buried oxide layer. In this new structure, the SPAD circuitry can be inscribed in the SPAD active area, and in combination with a back side illumination results in a high fill factor [7].

In our chosen SPAD configuration, the cathode is connected to a constant bias voltage while the P-well anode is the dynamic node. Despite its advantages, this

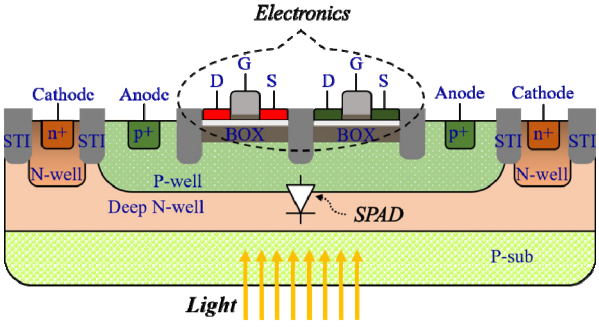

Fig. 1. A cross section of CMOS FDSOI technology. Integration of the SPAD and electronics in an inherent 3D structure with backside illumination (scales are not respected).

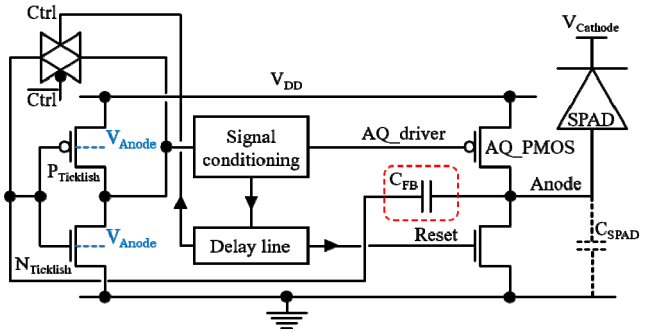

Fig. 2. Schematic of the Ticklish AQAR circuit. Bodies of all transistors are connected to anode voltage. For an indirect sensing C_{FB} must be removed.

configuration raises a serious problem. When an avalanche occurs, the anode voltage rises, this change modulates the threshold voltages of the transistors on top of the SPAD via the capacitive coupling through the buried oxide layer. In other words, the transistors undergo an undesired body biasing which depends on the SPAD anode voltage. Even though this body voltage change is an unwanted effect, in this paper we propose some circuits that take benefit from this effect and introduce a novel way of avalanche detection.

III. Ultra-Fast Active Quenching Circuit

As mentioned before, in order to reduce the AP effect, the number of charge carriers within the SCR during an avalanche should be minimized. This can be achieved by fastening the quenching process thanks to the AQ circuits.

A. Ticklish Inverter: A Novel Sensitive Detection Circuit

The efficiency of the AQ circuit mainly depends on how fast it can detect the avalanche. Therefore, in this paper we introduce a novel circuit, capable of promptly detecting the avalanche in its very first moments. Fig. 2 shows the schematic of the proposed circuit. The detection part is composed of an inverter and a T-gate named "Ticklish inverter". Using inverters to detect the avalanche has been reported in various works [1][11][12]. However, in most of these works; the inverter requires a large signal variation to toggle its output. This harshly degrades the sensitivity of the detection circuit and therefore the efficiency of the AP reduction. Although, by a proper sizing it is possible to reduce inverter threshold to some extent, but it is limited by the area consumption and parasitic capacitances of the inverter [11], which increase the AP and reduce the fill factor. However, in our proposed circuit, thanks to the "T-gate" feedback, the inverter is biased at its switching threshold. At this operating point, both NMOS and PMOS are on and in saturation, so the inverter actually acts as a high gain analog amplifier, not as a digital gate. The proposed circuit bypasses saturation regions on the inverter Voltage Transfer Characteristic (VTC) curve and only remains on the linear analog part, see Fig. 3. Therefore, a small signal variation, in the range of a very few millivolts at the input, results in a large signal variation at the output.

In the signal conditioning box (Fig. 2), two inverters are placed between the ticklish detector and the AQ transistor to convert the output of the detector to a binary signal, suitable for driving the AQ transistor, AQ_PMOS. After the quenching, a tunable delay line, resets again both the SPAD and the T-gate to makes the pixel ready for the next event. Thanks to the quick detection process which leads to a very

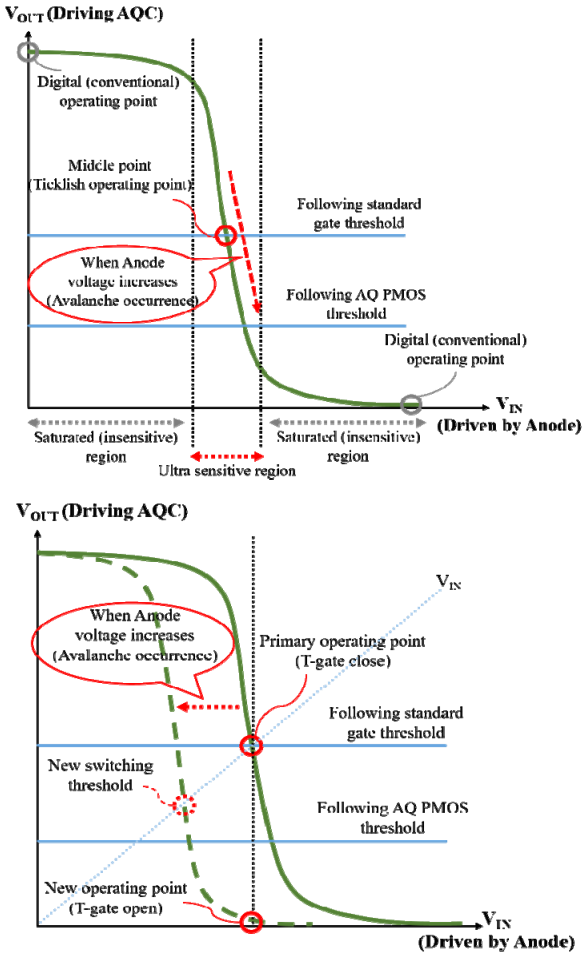

Fig. 3. VTC of the ticklish detector in direct sensing (top) and indirect sensing (bottom) demonstrating the concept of the ticklish detection.

fast quenching, the ticklish AQAR circuit is able to considerably reduce the total amount of charges that flow through the SPAD SCR.

B. Indirect Sensing: A New Way to Detect the Avalanche

It was pointed out that, by placing the electronics over the SPAD in FDSOI technology, the fill factor is no more limited by the embedded electronic, but the SPAD transient voltage affects the body of the transistors. If the "ticklish" AQAR circuit is fabricated over the SPAD and the coupling capacitor C_{FB} at the input of the ticklish inverter is removed, a new circuit is achieved, in which there is no wired connection between the detection circuit and the SPAD. In this new circuit the avalanche is only sensed through the body of the transistors of the Ticklish inverter. When the anode voltage starts to rise due to an avalanche, it decreases the NMOS threshold, increases the PMOS threshold and consequently pulls down the Ticklish inverter threshold, while it was biased at a higher threshold by the T-gate, see Fig. 3 (bottom). Thanks to the high sensitivity of the Ticklish detector, this small threshold decrease (80 mV/V) is enough for the detection of an avalanche.

In comparison with conventional direct sensing circuits, this novel indirect sensing circuit totally removes the wired connection between the SPAD and the detection circuit. This allows to strongly increase the excess bias of the SPAD as the body bias voltage can be adjusted to a range from -3 V up to +3 V in the targeted technology.

C. An Ultrafast and Compact SPAD Pixel

The combination of the ticklish detector in direct and the new indirect sensing method, results in an even faster detection since both the effects are added. The achieved inherently 3D, ultrafast AQAR circuit breaks the tradeoffs between the fill factor, the AP effect and the dynamic range. These proposed circuits are first ever reported AQAR circuits that exploit either direct or indirect sensing, or both sensing methods combined on a native 3D SPAD pixel.

IV. Post Layout Simulation Results

The proposed circuits have been designed and laid out in a 28 nm CMOS FDSOI technology. In Fig. 4 the layout of the Ticklish AQAR circuit in combined sensing mode is shown. The only difference between this layout and the layout of the ticklish AQAR circuit in indirect sensing mode is the coupling capacitance C_{FB}. The circuit occupies an area of about 14 µm × 14 µm, which is about 32 % of the area of our 28 µm diameter SPAD, therefore it can be completely placed over the SPAD, inside its active area. Most of the area is consumed by the delay line and there is still room to place more advanced signal processing circuits such as a counter or a compact time to digital converter. Along with a backside illumination the fill factor is not limited by the electronics and the pixel achieves the highest possible fill factor.

We used a Spice macro model for SPAD [13] to simulate the operation of the proposed circuits. The SPAD has a 100 fF junction capacitance and a 1 kΩ serial resistance. In order to measure the efficiency of the Ticklish AQAR circuits we compare all the results with the Passive Quenching (PQ) operation. To obtain more realistic results all simulations are made using post layout extracted schematic.

Fig. 5 shows the anode voltage when an avalanche occurs in active and passive quenching mode for both Ticklish AQAR circuits in combined sensing and indirect sensing. It is not possible to precisely determine when the avalanche is detected but in the anode voltage curve we can observe a slope change. This slope change means that after the avalanche detection, the circuit triggers the AQ PMOS to speed up the quenching. Therefore, surely the avalanche is detected in less than 50 ps in the combined sensing mode and in less than 100 ps for indirect sensing mode.

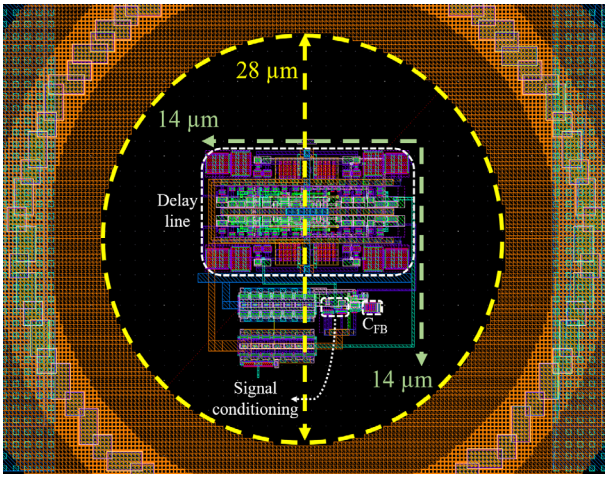

Fig. 4. Layout of the native 3D SPAD pixel. Ticklish AQAR circuit is inscribed in the SPAD active area.

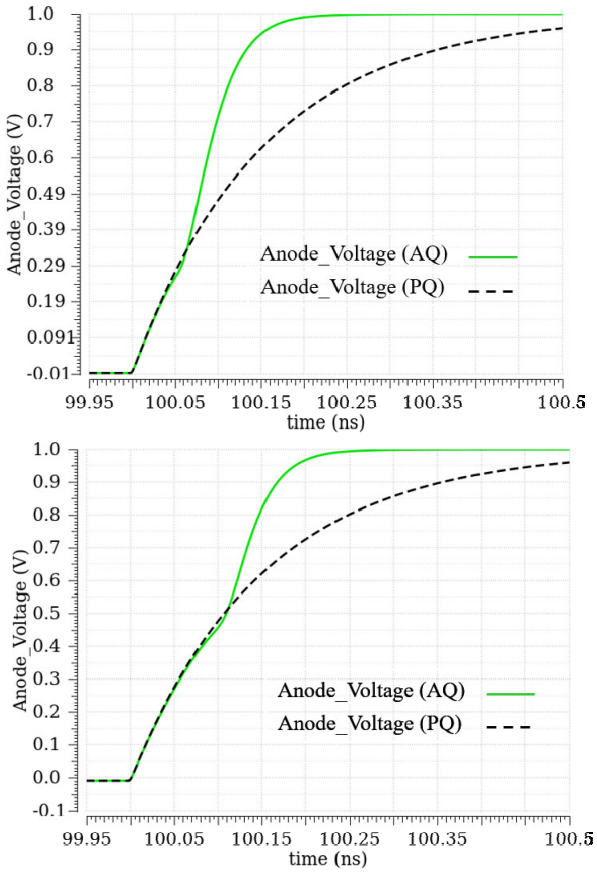

Fig. 5. Anode voltage variations when an avalanche occurs in both active and passive quenching modes. Direct+indirect sensing (top), indirect sensing (bottom).

Fig. 6 shows avalanche currents for both indirect and combined sensing circuits in active and passive quenching modes. As expected, a faster avalanche detection results in a faster quenching. According to Fig. 6, in the combined sensing circuit, the avalanche is actively quenched in about 200 ps while for the indirect sensing circuit, quenching time is about 240 ps. It should be noticed that the Ticklish AQAR circuit in combined and in indirect sensing mode quenches the avalanche respectively 3 times and 2 times faster than the corresponding passive quenching.

The surface under the avalanche current curve is equal to the avalanche charge in SCR. Fig. 7 is the result of taking integral from avalanche current curves in Fig. 6. The avalanche charge in SCR is reduced by 50 % and 30 %, respectively in combined and indirect sensing, regarding to the amount of the charge in PQ mode. It is observable in Fig. 7 that this reduction is due to the contribution of the AQ PMOS in the quenching process. Since there is a proportional relationship between the afterpulsing effect and the avalanche charge flowing through the SCR, Ticklish AQAR circuits in combined and indirect sensing should reduce the afterpulsing effect by 50 % and 30 % respectively.

V. Conclusion

In order to reduce the after pulsing effect, from a circuit design point of view, the avalanche charge flowing through the SCR should be reduced. In this paper an AQAR circuit based on an ultra-fast detection is proposed to speed up the quenching process and thus decreases the avalanche charge. Also with a novel inherent 3D SPAD pixel the circuitry does

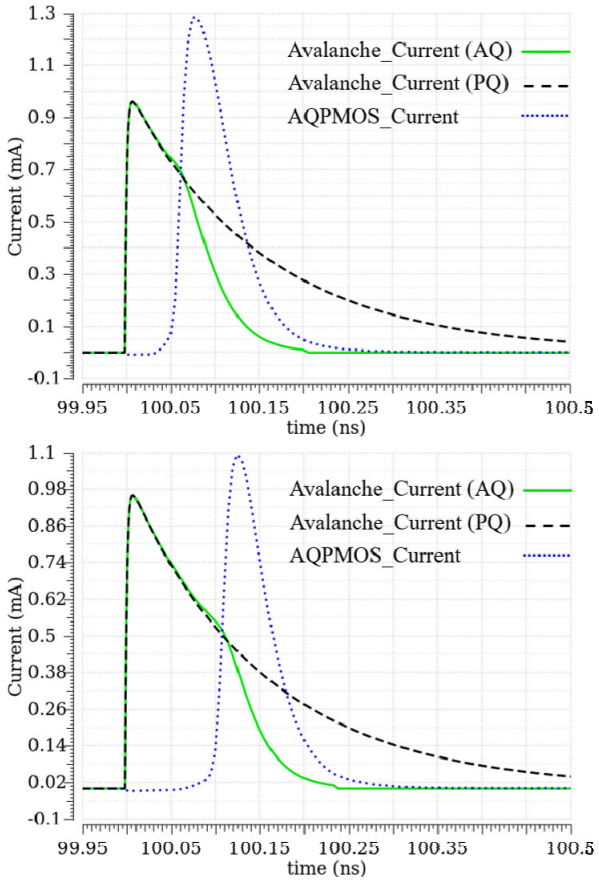

Fig. 6. Avalanche current and the current of active quenching transistor in both active and passive quenching modes. Combined sensing (top), indirect sensing (bottom).

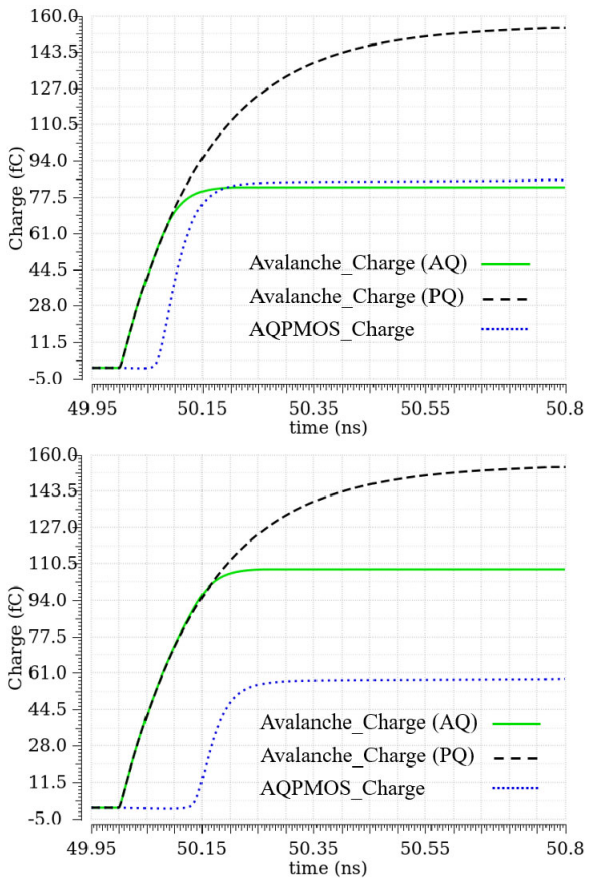

Fig. 7. Avalanche charge in SCR when an avalanche occurs in both active and passive quenching modes. Combined sensing (top), indirect sensing (bottom).

not affect the fill factor and keep it at its highest possible value. Post extracted simulation results show that the Ticklish AQAR circuit detects the avalanche in less than 50 ps and quenches it in about 200 ps, which results in a 50 % avalanche charge reduction and consequently 50 % afterpulsing reduction. Therefore, the proposed pixel bypasses conventional tradeoffs between the AP, the dynamic range and the fill factor.

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