Body-biasing considerations with SPAD FDSOI: advantages and drawbacks

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***Abstract* —This article focusses on Single Photon Avalanche Diodes (SPAD) integrated in CMOS UTBB FDSOI (Ultra-Thin Body and Box Fully Depleted Silicon-On-Insulator technology), as an original approach for natively 3D SPAD pixels. In parallel to the optimization of the SPAD performances, we discuss in this paper some design issues relative to body-biasing effects. The associated electronics placed on top of the SPAD is constrained: the well layer below the box must be a P-type then only regular threshold voltage NMOS and low threshold voltage PMOS transistors can be used. The SPAD avalanche events will affect the electronics through body-biasing effects that can be advantageously exploited for an indirect sensing of the SPAD activity. Then two simple indirect sensing cells are studied. Firstly, a voltage divider realized with two transistors in series (PFET and NFET operating as active resistances) is simulated and measured to demonstrate its ability to detect avalanches. Secondly, an even simpler cell is studied, as it consists of only one NMOS transistor configured as an equivalent capacitive bridge (gate and box capacitances). Finally, the advantages and disadvantages from a design point of view are addressed.**

Keywords — single photon avalanche diode (SPAD), CMOS, UTBB FDSOI, body-biasing, indirect sensing

I. INTRODUCTION

Single Photon Avalanche Diodes (SPAD) are widely used for low intensity light detection thanks to their high sensibility and ultra-fast response time [1-2]. SPADs can be easily integrated in CMOS technologies addressing many applications such as light detection and ranging, face recognition, 3D imaging, etc. For more demanding applications, 3D SPADs offer higher fill factor and photon detection efficiency but require a 3D-stacked chip process [2]. In this context, an original approach for a native 3D pixel has been proposed with the integration of SPAD in CMOS UTBB (Ultra-Thin Body and Box) FDSOI (Fully Depleted Silicon-On-Insulator) technology [3-4]. Preliminary results demonstrated the correct operation of the diode in Geiger mode, nevertheless a low breakdown voltage V_{BD} associated with band-to-band and field-enhanced trap assisted tunneling effects limited the operating range to low excess voltage [4]. Ongoing work focuses on the optimization of the diode junction to increase V_{BD} [5]. In this article, the coupling between the SPAD and its associated electronics on top of the BOX is studied. Body-biasing, which is the key feature of CMOS UTBB FDSOI platform for performance-consumption tradeoffs [6], plays an important role when integrating SPAD in CMOS FDSOI. In the following sections, some benefits (e.g. indirect sensing of SPAD avalanche events) and drawbacks (e.g. constraints in the embedded electronics on top of SPAD) are discussed and illustrated.

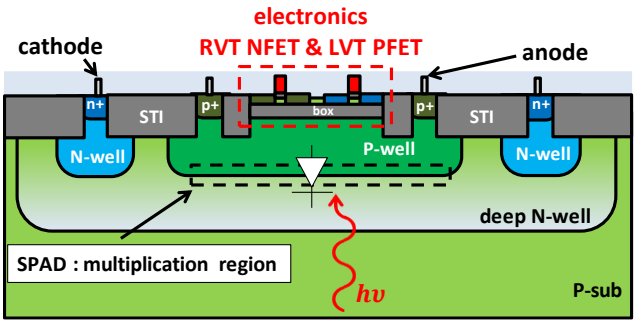

Fig. 1. Schematic cross section of SPAD implemented in CMOS FDSOI technology (scales are not respected). As electronics is placed on top of P-well layer (SPAD anode), only regular V_{th} NFET and low V_{th} PFET can be used.

II. SPAD IMPLEMENTED IN CMOS FDSOI TECHNOLOGY AND ASSOCIATED ELECTRONICS AS A 3D PIXEL

A. SPAD FDSOI architecture

In Fig. 1, the schematic cross-section of SPAD FDSOI is presented: the diode is realized with deep N-well and P-well layers below the ultra-thin buried box ($25\,nm$) while the associated electronic circuits are placed on top, integrated in the thin silicon film ($7\,nm$). This allows a native 3D pixel using backside illumination with improved performances such a

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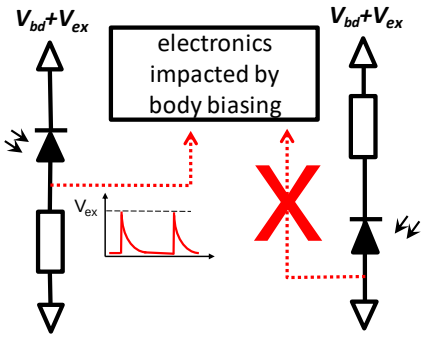

Fig. 2. SPAD configuration. Left: SPAD on top, SPAD anode (P-well layer) voltage will vary according to avalanche events, due to body-biasing effects. Right: SPAD on bottom, anode is grounded or biased at a constant voltage, no body-biasing effect in this case.

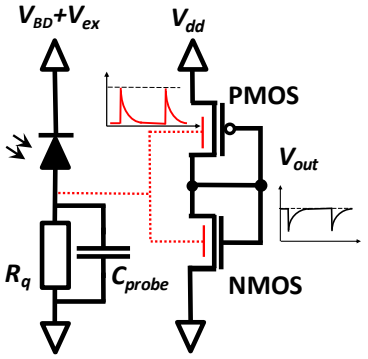

Fig.3. Indirect sensing cell built with a voltage divider realized with two transistors in series (PFET and NFET operating as active resistances).

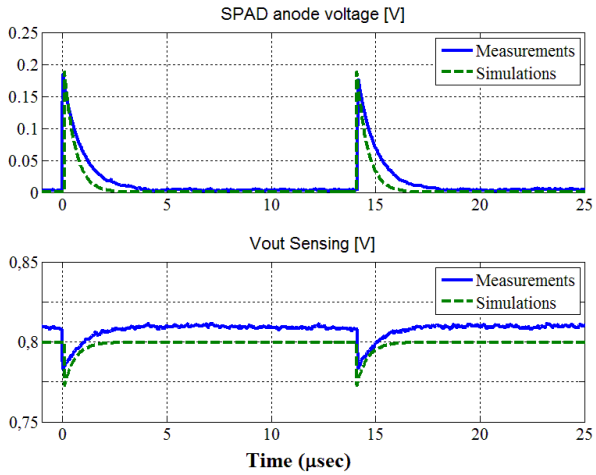

Fig.4. Measurements and simulations of the voltage divider used an indirect sensing of SPAD avalanches (excess voltage above breakdown voltage: $V_{ex} = 0.2\,V$, $R_q = 200\,k\Omega$).

higher fill factor with an optimized photon detection efficiency for near infrared light. One important remark regarding the electronics on top of SPAD FDSOI is the loss of flexibility in the different transistor flavors: only regular V_{th} NMOS (RVT NFET) and low V_{th} PMOS transistors (LVT PFET) can be used, otherwise the electronics cells have to be placed outside SPAD area.

B. *Body-biasing effects depending on SPAD configuration*

As illustrated in Fig. 1, the embedded electronics above the SPAD is capacitively coupled to the P-well (the SPAD anode) through the thin buried oxide - BOX ($25\,nm$), and is therefore subjected to body-biasing effects, depending on the SPAD configuration. One can consider two cases (Fig. 2). First case, SPAD is placed on top and quenching element (e.g. resistor) connected to the anode. In this case, P-well voltage varies according to avalanche events and therefore the electronics may be impacted. In the second case, the quenching element is connected to the cathode, while the anode is at a constant bias, and consequently, no body-biasing effect will occur. The second case appears preferable, nevertheless when considering a SPAD matrix, the fill-factor will be maximized when merging all the diodes in the same deep N-well (first case presented previously). Then the body-biasing analysis with SPAD FDSOI is of the highest importance to highlight possible design issues. In the following sections, only the configuration where the SPAD is on top will be considered, i.e. the SPAD anode voltage (P-well) varies according to the SPAD activity (SPAD matrix configuration in perspective).

III. Body-Biasing Induced by SPAD Activity

A. *Impact on logic gates*

As mentioned in the previous section, available standard cells cannot be placed on top of SPAD FDSOI as only RVT NFET and LVT PFET can be used (Fig. 1). Thus, a full standard cell library needs to be rebuilt. The impact of SPAD activity onto the logic functionality also has to be analyzed deeply. Each SPAD avalanche dynamically modifies the threshold voltage of transistors, changing the transfer characteristic of the gates. In practice, an avalanche event leads to a positive transient voltage pulse on the anode (P-well voltage increase). Then, during the avalanche transient, the NMOS threshold voltage $V_{th,n}$ decreases (forward body-biasing) while the absolute value of the PMOS threshold voltage $|V_{th,p}|$ increases (reverse body-biasing). For this reason, robustness on the logic circuitry (placed on top of SPAD FDSOI) during avalanche transient has to be evaluated. In next section, body-biasing is advantageously exploited for indirect sensing of the SPAD activity.

B. *Body-biasing used for indirect avalanche sensing*

In this section, two simple approaches for indirect sensing of the SPAD activity are presented (i.e. no physical connection to the SPAD anode), thanks to the body-biasing effects.

1) *Voltage divider as sensing cell*

The first sensing cell (placed on top of the SPAD) is composed of two active resistors in series (as shown in Fig. 3) with the output node as the middle point of the voltage divider. In order to enhance the body-biasing effect, we chose thick oxide transistors (named GO2 oxide or EG family, for "Extended Gate"). They present a larger body-bias factor ($\Delta V_{th}/\Delta V_{bb} \sim 140\,mV/V$). When SPAD avalanche occurs, a

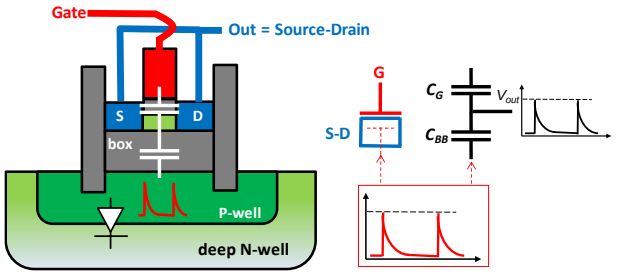

Fig. 5. Principle of the capacitive sensing cell with a single transistor (e.g. regular V_{th} NFET). Left: schematic-cross-section of the transistor (source and drain are connected together). Right: equivalent model with two capacitors in series C_G and C_{BB}.

positive transient signal on the P-well will affect the transistors: the equivalent resistance of the NFET will decrease (forward body-biasing), while the one of the PFET will increase (reverse body-biasing). Consequently, a transient peak is observed in Fig. 4, where experimental and simulated signals are superimposed. Simulations are obtained with a behavioral SPAD model (based on [7]) and the transistor model available in the physical design kit - PDK (based on [8]). SPAD anode voltage and middle point of the divider were simultaneously measured with active probes. The relatively long time constant is due to the quench resistance ($\sim 200\ k\Omega$) and the equivalent capacitance (pad and the active probe: $\sim 3\ pF$). From the results presented in Fig. 4, it is evident that the indirect detection of the avalanche events is possible by using this cell.

2) Capacitance-NFET as sensing cell

The second detection circuit is even simpler because it consists of only one NMOS transistor (regular V_{th} with thick oxide - GO2) in an equivalent capacitance configuration (i.e. source and drain are connected together). Fig. 5 illustrates the schematic of the NMOS transistor on top of the SPAD and its equivalent capacitive divider, composed of the gate channel and the back-biasing capacitances respectively named C_G and C_{BB}. This sensing cell was simulated with the available transistor model in the PDK [8] varying its size ($L \times W$). Thanks to the ultra-thin box (25 nm [6]), the capacitive divider allows sensing a SPAD avalanche event, as it is demonstrated in the next section.

3) Simulation of the sensing cells

The whole simulation schematic, including the SPAD behavioral model and the two sensing cells is presented in Fig. 6: *i)* the resistive divider (PFET and NFET as active resistors in series), *ii)* the capacitive divider (NFET with the source and drain connected together) and buffers. The red dashed line represents the indirect sensing path, i.e. the P-well layer (SPAD anode). In Fig. 7, several impinging photons were simulated. The SPAD anode voltage was plotted: its peaks present magnitude approximately equals to the excess voltage above the breakdown voltage and are linked to the avalanche events. The resistive divider voltage (middle point voltage, V_m) and the capacitive divider voltage (source-drain voltage, V_{S-D}) are also represented. The shapes of these two waveforms are complementary (negative peak versus positive peak). One can notice that the output peak-to-peak magnitudes for both sensing

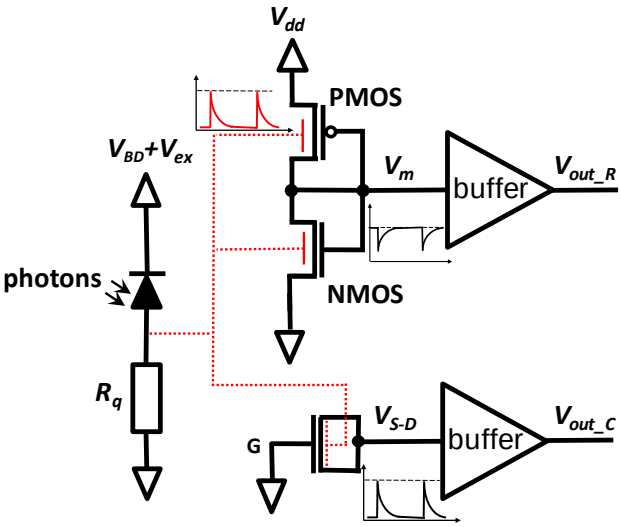

Fig.6. Simulation schematic with the SPAD and the two indirect sensing circuits: resistive and capacitive dividers (NFET with the source and drain connected together).

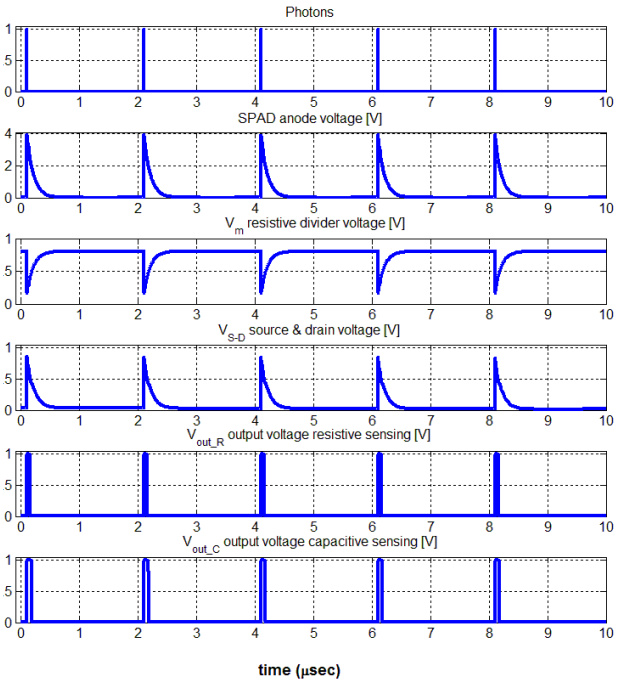

Fig. 7. Simulation results of the scheme presented in Fig. 6 (excess voltage above breakdown voltage: $V_{ex} = 4\ V$, $R_q = 200\ k\Omega$).

cells are almost identical (linked to the body-biasing factor). The last two curves (V_{out_R} and V_{out_C}) represent the output voltages after the buffers. Both indirect sensing cells seem interesting. The capacitive divider (only simulated at the moment) presents quite a large area (minimum NMOS size: $L \times W \sim 4\mu m^2$) and a negligible static power consumption, while the resistive divider (experimentally validated in section III.B.1) occupies less area but presents a static consumption around $100\ \mu W$.

IV. Conclusion

Single Photon Avalanche Diode implemented in CMOS UTBB FDSOI technology provides an intrinsic 3D pixel with the diode placed below the buried oxide and its associated electronics on top. In this article, we discuss some advantages and drawbacks of such an architecture. The first point to be considered is related to the logic cells on top of SPAD FDSOI that can only be constituted with regular V_{th} NFET and low V_{th} PFET, excluding the use of the standard logic cell libraries, already available in the physical design kit. Additionally, in order to achieve a compact SPAD matrix, the most interesting architecture should be a common deep N-well (SPAD cathodes) with isolated SPAD anodes (P-well below the buried oxide), introducing body-biasing effects during avalanche transients. Indirect SPAD activity sensing is possible, offering innovative circuitry for quenching. Indeed, a SPAD avalanche event will induce a positive voltage peak in the P-well layer, its magnitude approximately equals to the excess voltage above the breakdown voltage. This voltage transient peak will affect the electronics above that can be advantageously exploited for an indirect sensing of the SPAD activity.

Then two indirect sensing cells were presented. The first one (experimentally demonstrated) relies on an active resistor divider, built with thick oxide transistors. The second cell is even simpler (consisting of only one NMOS transistor: regular V_{th} with thick oxide) in an equivalent capacitive divider. The latter is composed of the transistor gate capacitance (its source and drain are connected together) and the body-biasing capacitance. Both sensing cells present interesting behaviors with a tradeoff between occupied area and static power consumption. Indirect SPAD FDSOI activity sensing is then demonstrated, offering innovative circuitry for quenching. Additional work is underway to validate the different approaches, firstly with additional simulations and in, a second step, with a new test chip. In parallel, a study is carried out on the improvement of the intrinsic performances of the SPAD FDSOI.

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